CURRICULUM VITAE

Dr. M. Maheswari, M. Tech., Ph.D
G2- AA, 26, Sivaprakasam salai,
Anna nagar, Tenur
Trichy-620 017.

Field of Specialization:
VLSI based System Design, System design on reconfigurable device and ASIC, Design of custom Topology for Network-on-Chip, Design of error control codes for Network-on-Chip.

Academic Record

Degree	Specialization	Institution	Marks	Year
Ph. D	VLSI System	Anna University, Chennai	----	2009-2014
M. Tech.,	VLSI System	National Institute of Technology (NIT), Trichy	7.7 (CGPA)	2002- 2004
B.E	ECE	Bharathiar University, Coimbatore	73%	1992-1996

Ph. D Thesis Title: NOVEL APPROACHES IN THE DESIGN OF RELIABLE CUSTOM TOPOLOGY FOR APPLICATION SPECIFIC NETWORK-ON-CHIP

Teaching and Research Experience

Institution	Designation	Year	Experience in years
Shri Angalamman College of Engineering and Technology, Trichy	Lecturer	17-12-1997 to 30-10-2003	5 years 10 months
J.J College of Engineering and Technology, Trichy	Senior Lecturer to Professor	31-10-2003 to 31-12-2014	11 years 2 months
K. Ramakrishnan College of Engineering, Trichy	Professor	02 - 01- 2015 To Till date	6years 3 month
Total			**23 years 4 month**

Carrier Summary

- **21 years** of teaching experience as Lecturer/Asst. Professor/Professor in the department of Electronics and Communication Engineering.
- **Anna University, Chennai Recognized Supervisor (2540048)**
- Published **2 papers in SCI journals (Elsevier, Springer) 6 papers in Scopus indexed journal.**
- **Published more than 30 papers in reputed journals/International Conferences/National conferences.**
- Achieved more than 90% results and obtained 95% positive feedback from the students in all the semesters.

- Presented many research papers in national / international conferences and journals.
- Received cash awards three times, for producing 100% results and more than 95% results.
- Honored as chair person for a International Conference conducted at J.J College of Engineering and Technology, held on 13 & 14 December-2012.
- NAAC coordinator and got NAAC 'A' Grade at K. Ramakrishnan college of Engineering, Trichy.
- NBA department coordinator and got NBA accreditation in the year 2019

Grant Received

- **Received a sum of Rs. 9,500 project** from TNSCST for student project scheme.
- **Received fund of Rs. 15,000 from TNSCST to** organize program on "Popularization Science Activity"
- **Received Rs. 20,000 fund** from DST NIMAT to conduct Entrepreneurship Awareness camp at K. Ramakrishnan College of Engineering in the year 2017.
- **Received Rs. 40,000 fund** from DST NIMAT to conduct Entrepreneurship Awareness camp at K. Ramakrishnan College of Engineering in the year 2018.
- **Received Rs. 20,000 fund** from DST NIMAT to conduct Entrepreneurship Awareness camp at K. Ramakrishnan College of Engineering in the year 2019.
- **Received fund of Rs. 10.7 lakh from AICTE under the scheme of MODROB in the year 2020**
- **Received fund of Rs. 5,40,925 for FDP on " Challenges and Design Techniques of Machine learning Techniques for Cyber Physical Systems" in the year 2020**

Administrative Responsibility held

- Head of the department of ECE at JJ college of Engineering and Technology, Trichy for 14 months. 14-11-2013 to 31-12-2014.
- Faculty in-charge for setting up new VSLI laboratory JJ college of Engineering and Technology, Trichy.
- Faculty in-charge for department association at JJ college of Engineering and Technology, Trichy.
- Technical committee convener for the International Conference "INCOSET 2012" held on 13-12-12 to 14-12-12 at JJ college of Engineering and Technology, Trichy.
- Organized Two National Conferences at JJ college of Engineering and Technology, Trichy in the year 2013 and 2014.
- Attendance cell Coordinator at JJ college of Engineering and Technology, Trichy
- NBA coordinator JJ college of Engineering and Technology, Trichy.
- NAAC coordinator in KRCE.
- NBA department coordinator and got NBA accreditation in the year 2019

Software Tools known/Worked

- Cadence Analog and Digital Design Tool
- Xilinx/ Altera FPGA design Tool
- Advanced Design System.
- Multisim Tool.

Certificates Obtained

- Received **"Elite" certificate from NPTEL- for online course for the subject Principles of modern CDMA/ MIMO/OFDM wireless communication.**
- **Received "Elite" certificate from NPTEL- for online course for the subject hardware modling using verilog HDL.**

Guidance of Master's Thesis

Master's thesis guided - 25

SUBJECT TAUGHT

UNDER GRADUATE

VLSI design, Linear Integrated circuits, Digital System Design, Microprocessor and micro system, Electron Devices, Electronics circuits I &II, Computer Networks, High speed Networks, Wireless communication. Wireless networks

POST GRADUATE

ASIC design, VLSI design, DSP IC, VLSI signal processing, DSP architecture and its applications, VLSI architecture and design methodology, Three dimensional NOC Low power VLSI

Membership of Professional Bodies

- Life member, Indian Society for Technical Education (MISTE) India (LM 67201)
- Life member, Broadcast Engineering Society, (BES)

Seminars/Workshops/Symposium Organized

- Organized National conference on March 14th 2014 at JJCET, Trichy
- Organized Two day National level workshop on "Emerging wireless technology and Its CAD tools" on February 12th & 13th 2016 at KRCE
- Organized one day National level seminar on "Internet of Things" February 24th -2016 at KRCE
- Organized two days workshop Emerging wireless technologies on September 2016 at KRCE
- Organized one day IETE sponsored Technical Symposium on 9th March2017 at KRCE
- Organized DST NIMAT sponsored three days Entrepreneurship awareness camp at K. Ramakrishnan College of Engineering during 9th -12th August, 2017
- Organized DST NIMAT sponsored three days Entrepreneurship awareness camp at K. Ramakrishnan College of Engineering during 20th – 22nd August, 2018
- Organized TNSCST sponsored workshop on " Personal and Menstrual hygiene for Rural woman for Samayapuram and nearby villages"
- Organized DST NIMAT sponsored three days Entrepreneurship awareness camp at K. Ramakrishnan College of Engineering during 4th – 6th February, 2019

Short-Term Courses/Conferences/Seminars/Workshops Attended

- Short-Term Courses/Workshops: 10
- Seminars: 05
- International Conferences : 07
- National Conferences : 08

Guest Lectures Delivered -03

- Delivered a Guest lecture on "***Evolution of Digital Integrated Circuits***" at Adhiyaman college of Engineering, Hosur,
- Delivered a Guest lecture on " ***Testing of VLSI*** " in Faculty Development Program at Oxford Engineering College, Trichy.
- Delivered a Guest lecture on " **Reliability of interconnects in Network-on-Chip**" in AICTE sponsored STTP at Oxford Engineering College, Trichy.

REVIEWER

- IEEE Transaction on VLSI system
- IEEE Access

Patents Filed

1. **Application no. and date: 201841015156 & 21/04/2018**
   Title : Apparatus for determining temperature and level of liquid in a closed container
2. **Application no. and date: 201841010937 & 25/03/2018**
   Title: Methods and systems for making use of helmets mandatory
3. **Application no. and date: 201941003312 , 28/01/2019**
   Tile: AQUACULTURE MONITORING SYSTEM
4. **Application no. and date: 201941003309 , 28/01/2019**
   Title: A WASTE MANAGEMENT SYSTEM
5. **Application No.202041037311 A Date: 11/09/2020**
   Title: A NOVEL APPROACH OF BIOMARKER DETECTION BY OPTICAL HIGH SENSITIVITY NANO

Patents Published

1. **Application no. and date: 201841015156 & 21/04/2018**
   Title : Apparatus for determining temperature and level of liquid in a closed container
2. **Application no. and date: 201841010937 & 25/03/2018**
   Title: Methods and systems for making use of helmets mandatory
3. **Application no. and date: 201941003312 , 28/01/2019**
   Tile: AQUACULTURE MONITORING SYSTEM
4. **Application no. and date: 201941003309 , 28/01/2019**
   Title: A WASTE MANAGEMENT SYSTEM

PATENT GRANTED:

1. (Australian Patent) Soil Health Monitoring Using Drones and Augmented Reality in Agricultural Regions

Research Publications

Total Citations: 89
i10 index : 1
h index: 5

Book chapter -01

1. **M.Maheswari and** G.Seetharaman, 'Implementation of Application specific Network on chip Architectures on Reconfigurable Devices using Topology Generation Algorithm with Genetic Algorithm based optimization Technique' K.R Venugopal and L.M Patnaik (Eds.): ICIP 2012, CCIS 292, pp. 436–445, 2012. Springer-Verlag Berlin Heidelberg 2012. **(Anna university - Annexure II, SNIP-0.247).**

International Journals- 10

1. **M.Maheswari and** G. Seetharaman**,** 'Multi bit Random and burst error correction code with crosstalk avoidance for reliable on chip interconnection links' Microprocess. Microsyst. Vol. 37, No. 4-5, pp.420-429, 2013. (**SCI - Elsevier Journal**, Anna university-**Annexure I, IMPACT FACTOR- 0.598).**
2. **M.Maheswari and** G.Seetharaman, 'Enhanced Low Complex Double Error Correction Coding with Crosstalk Avoidance for Reliable On- Chip Interconnection Link', Journal of Electronic Testing-Theory and Applications (JETTA)- **Volume 30, Issue 4 (2014), Page 387-400,** (**SCI - Springer journal**, Anna university-**Annexure I, IMPACT FACTOR- 0.475).**
3. **M.Maheswari and** G.Seetharaman, 'Hamming Product Code Based Multiple Bit Error Correction Coding Scheme Using Keyboard Scan Based Decoding for On Chip Interconnects Links' Applied Mechanics and Materials Journal, Vols. 241-244, pp. 2457-2461, 2013. **(Anna university -Annexure II, SNIP-0.270). (Scopus Indexed)**
4. **M.Maheswari and** G.Seetharaman, 'Design of a novel error correction coding with crosstalk avoidance for on hip interconnection link', Int. J. Computer Applications in Technology, Vol. 49, No.1, pp. 80-88, 2014. **(Anna university -Annexure II, SNIP-0.487). (Scopus Indexed)**
5. N.Latha, **M,Maheswari**, Dr. T.N.Prabhakaran,"Multi bit error correction scheme based on Keyboard scan decoding for NoCs with type II hybrid ARQ" **International Journal of Communications and Engineering**, Vol. 2, no.2, Issue 4, March-2012.
6. **M.Maheswari** , " A Novel Custom Topology Generation for Application Specific Network on chip using Genetic Algorithm optimization Technique" **Journal of Artificial Intelligence**, Vol. 6(1), pp.8-21, 2013. **(Anna University-Annexure II, SNIP-1.96) (Scopus Indexed)**
7. **M.Maheswari** and V. Srinivasan**,** "New Methodology for the Enhancement of Spectral Amplitude Coding – Optical Code Division Multiple Access (SAC–OCDMA) System & its Performance Measures", International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE) ISSN: 0976-1353 Volume 7, Issue 1, pp. 207-210, 2014.
8. R. Shifana Patch and **Dr. M. Maheswari, "**Artificial Neural Network Based Smell Simulator for Visualization" International Journal of Students' Research In Technology & Management, Vol. 3(4), pp. 328-329,April, 2015.
9. **Dr. M. Maheswari**, T. Margret Rosy, " Design of an Improved Finite Impulse Response (FIR) filter using Vedic multiplier", CiiT International Journal of Programmable Device circuits and systems", Vol.7, No.4,pp. 113-118 , April-2015.

10. **Dr. M. Maheswari,** "Design of Reliable custom topology for Application Specific Network on chip", International Journal of Advanced Research in Electrical and Electronics and Instrumentation Engineering (IJAREEIE) Vol. 4, Issue 5, pp. 4039-4046, May 2015.

11. Hemalatha.B , **M.Maheswari** & Balamurugan.R " Design of Cascaded Integrator Comb Filter for Signal Processing Application" International Journal of Applied Engineering Research, ISSN 0973-4562 Vol. 10 No.20 , pp. 20011-20014, (2015) **(Scopus Indexed)**

12. Vimal. S, **.M.Maheswari** "Improved Design of RF BJT Low Noise Amplifier for 5 to 6 GHz Frequency Range" International Journal of Applied Engineering Research, ISSN 0973-4562 Vol. 10 No.20 , pp. 19970- 19973, (2015) **(Scopus Indexed)**

13. Ramya S, **.M.Maheswari** & Saranya J "Design of Frequency Reconfigurable low profile Patch Antenna" International Journal of Applied Engineering Research, ISSN 0973-4562 Vol. 10 No.20 , pp. 20007-20010, (2015) **(Scopus Indexed)**

14. Vimal. S, **M.Maheswari "**Design and performance improvement of a low noise amplifier with different matching techniques and stability network" International Journal of Engineering Research & Science, Vol-2, Issue-3, pp. 1-10, March- 2016.

15. Ramya, M. Maheswari,"Design of Frequency Reconfigurable antenna using Varactor Diode,"International journal ssrg, April-2016, PP.136-139, ISSN 2348 8549

16. Gayathri R, Maheswari M, " Design And Fabrication Of Dual Band Rfid Antenna Using Hybrid Coupler With CSRR", Pakistan Journal of Bio Technology, Vol 14(1), pp. 87-89, 2017 (**Scopus/Annexure** II)

17. M. Maheswari*, R. Gayathri and S. Vimal, "Design And Performance Analysis Of Low Noise Amplifier With Filters For Wban Based Health Monitoring System", Pakistan Journal of Bio Technology, Vol 14(1), pp. 849-54, 2017 (**Scopus/Annexure** II).

18. S. SthiyaPriya and M. Maheswari, "Low-power area efficient reconfigurable multiplier architecture for FIR filter" IEEE Xplore : DOI: 10.1109/CESYS.2017.8321160 (**Scopus)**

19. Indumathi R., Maheswari M. (2018) Diagnosis of Cardiovascular Diseases (CVD) Using Medical Images. In: Bhuvaneswari M., Saxena J. (eds) Intelligent and Efficient Electrical Systems. Lecture Notes in Electrical Engineering, vol 446. Springer, Singapore. (**Scopus)**

20. M.Maheswari, B. Murugeshwari, "Random and Triple burst error correction code with low redundancy for Network-on-Chip link", DOI: 10.1109/CESYS.2017.8321160 (IEEE XPLORE)

21. N. Radha, M. Maheswari. " High speed efficient multiplier design using reversible gates", IEEE xplore pp-1-4 January 2018. **(Scopus)**

22. G.S. Sankari, M. Maheswari, "Energy Efficientweighted Test Pattern Generator Based BIST Architecture", I-SMAc-2018-IEEE Xplore- 2018.

23. N. Radha and M. Maheswari ," An Efficient Implementation of BCD to Seven Segment Decoder using MGDI", I-SMAc-2018-IEEE Xplore- 2018.

24. M. Banupriya, M. Maheswari," Multicarrier Modulation For 5g Mobile Applications", *IOSR Journal of Electronics and Communication Engineering (IOSR-JECE), pp. 1-5*

25. T. Muruganantham, M. Maheswari, "A Survey on Ultra Wide Band and Narrow Band Low Noise Amplifiers for Wireless Transceivers" International Journal of Advanced Research in Computer and Communication Engineering, Vol. 8, Issue 5, May 2019

26. V.Subhashini, Dr.M.Maheswari, A.Abinaya, "Design of Active Inductor Based Tunable Low Noise Amplifier (LNA)", Vol. 8, Issue 5, May 2019.

27. R. Kavipriya, M. Maheswari, "High Speed Polar Encoder Architecture For next Generation 5G Applications Using Radix-k Processing Engine" (ICCCI -2019), IEEE Xplore -2019 (Scopus)

28. N, Radha and M, Maheswari and P, Muralikrishnan, An Efficient Implementation of Hybrid Carry Select Adder Using Parallel Prefix Addition and Binary to Excess 1 Conversion (August 1, 2019). Proceedings of International Conference on Recent Trends in Computing, Communication & Networking Technologies (ICRTCCNT) 2019. Available at SSRN: https://ssrn.com/abstract=3430593 or http://dx.doi.org/10.2139/ssrn.3430593

29. Abinaya, M. Maheswari, Abdullah Saleh Alqahtani, "Heuristic Analysis of CIC Filter Design for Next-Generation Wireless Applications", Arabian Journal for Science and Engineering, https://doi.org/10.1007/s13369-020-05016-1 (SCIE)

International Conferences

1. **M.Maheswari and G.Seetharaman**, 'Design and implementation of Low Complexity Router for 2D mesh Network On Chip using FPGA' In the proce. Of International conference on Embedded system application' Los vegas, USA, July-18th -21st , 2011.
2. **Sarithra and M. Maheswari** "Design of Non-linear Trellis code for BIBO Multiple Access channel using single user Decoding" ICMEET-2k13, pp.625-632, 2013.
3. **Brinda and M. Maheswari "**Memory Efficient Arithmetic Architecture for SPHIT" ICACT-2013, ISBN 978-93-80757-74-2, 8 & 9th March-2013.
4. **Ranjana Priya and M. Maheswari** "Comparison of CORDIC and improved CORDIC design for satellite communication" ICRTET 2014, Mount Zion college, ISBN No. 978-93-5137-551-7, pp. 333-337, March 13 & 14, 2014.
5. **Margret Rosy and M. Maheswari** " Design of FIR filter using Vedic multiplier" International conference TITCON'14 at AVS engineering college, Salem, 8-9th April-2014.
6. **Ramya s, M. Maheswari , "**Design of Frequency reconfigurable antenna using Varactor diode" in International conference ICEJS-2016 on April- 22nd 2016.
7. **Indhumathi R, Maheswari M, "**Diagnosis of cardio vascular diseases using medical images" Second International conference – ICIEES-2017 at PSG college of Technology, Coimbatore on 20-21 January 2017.
8. Sathiyapriya, M. Maheswari, " Low power area efficient multiplier architecture for FIR filter", 2nd International Conference ICCES-2017 at PPG institute of Technology, during 19th -20th October 2017

NATIONAL CONFERENCE

1. **M.Maheswari** "*MIMO-OFDM transceivers for WLAN" in the proceeding of National conference conducted at Adhiyaman College of Engineering, Hosur, 6-7 March'2006.*

2. **M.Maheswari "** Mobile Wimax" in the national conference RETREW'08 at TKM Institute of Technology, Kollam,Kerala, 12th March 2008.
3. **M.Maheswari** " Wimax BWT and its performance Evaluation" in the National Conference conducted at Anna university-Chennai, 8th May 2008.
4. G.SHEEBA, **M.Maheswari** "Design and Implementation of Adaptive Median Filter On Reconfigurable Device" in the proceeding of National conference conducted at Kamaraj College of Engineering and Technology, Viruthunagar, Tamilnadu.
5. R.SHALINI, **M.Maheswari "** Design of a router for Network on chip architecture on Reconfigurable Device" in the Proceeding of National Conference conducted at Sivanthi Adithanar College of Engineering, Thiruchendur, Tamilnadu.
6. NOORJAHAN, **M.Maheswari** " Power optimization for NoC by Network Prtitioning: A topology Based Approach" in the Proceeding of National Conference conducted at Anna university of Technology, Trichy, Tamilnadu., March- 2011
7. SARANYA, **M.Maheswari** "Design and performance Analysis of router for NoC using Queuing Analysis" in the Proceeding of National Conference conducted at Anna university of Technology, Trichy, Tamilnadu.,March- 2011
8. Margret Rosy and **M.Maheswari** " Design of High speed Vedic multiplier" National conference conducted in K. Ramakrishnan college of Engineerign, Trichy, April-2014
9. Vimal s, M. Maheswari , "Design and Performance Improvement of LNA with matching techniques and stability networks", at National conference –ICVE-2016 on March 16th & 17th 2016.