**Researcher: Dr. P. Senthil**

Research profile: He holds Ph.D. from Anna University in VLSI design. His research domains are in the area of hardware design for arithmetic, hardware security and computer architecture.

**Profile**

**Education:**

**PhD ( V L S I ) Information and Communication Engineering. Jun 2014 to Feb 2021**

Anna University, Chennai, India.

*Dissertation title:* "Design and Implementation of Subnormal Floating-point SoC for Secured SignalProcessing using Pipeline Interconnect"

**ME VLSI design (PT)- 7.76 CGPA** **2012**

Oxford Engineering College, Trichy- Affiliated to Anna University, Chennai

**BE Computer Science Engineering- 68%** **2007**

M. Kumarasamy College of Engineering, Karur- Affiliated to Anna University, Chennai

**Diploma in Electronics and Communication Engineering – 77.5%** **2000**

Government Polytechnic, Trichy

**SSLC – 87 %** **1997**

Marist High School, Karur

**Experience:**

- Design and research experience (June 2014 to Feb 2021)-Floating point data path SoC for subnormal processing with microarchitectural design
- Teaching experience (Dec 2011 to Dec 2018) as assistant professor in Electronics and Communication Engineering, Chettinad College of Engineering and Technology Karur
- Freelance in Hardware design and VLSI (Jan 2019 to Mar 2022)

**Papers presented (Journal and conference)**

**P.Senthil** and Dr.VE.Jayanthi, "**Alleviation of Data Timing Channels in Normalized/Subnormal FloatingPoint Multiplier" Journal of Circuits, Systems and Computers**, World Scientific Publisher. Vol. 30, No. 1(2021), World Scientific Publishing Company. **DOI:10.1142/S0218126621200012 2120001** (24 pages). **(Indexed SCI-E IF: 1.369)**

Dr.VE.Jayanthi, **P.senthil**, "**Design a hybrid VLSI architecture for visible digital image watermarking in spatial and frequency domain" Journal of Circuits, Systems and Computers**. World Scientific Publishing Company. Published online: **DOI:10.1142/S0218126622500207**. Vol. 31, No. 2 (2022 Jan). **(Indexed SCI-E IF: 1.369).**

A.Kavitha, Anusiya saral and **P.Senthil**, **"Design Model of Retiming**

**Multiplier For FIR Filter & its Verification" International Journal of Pure and Applied Mathematics,** Volume 116 No. 12 2017, 239-247. **(Indexed in scopus) DOI: 10.12732/ijpam.v116i12.25**

**P. Senthil**, P.Saravanan, Dr. Utku KOSE, Sudhir Kumar Sharma and K. Vijayakumar, **"Resource Efficient Embedded Floating Point Unit with Microarchitectural State Implementation in FPGA" Microprocessor and Microsystems**, Elsevier, Submitted on Jan 2021, **Status-review completed as on 10.03.2021. (Indexed in SCI-E, IF: 1.139)**

**P.Senthil,** P.Saravanan, **"Area-Latency Efficient Floating Point Adder using InterleavedAlignment and Normalization" Integration the VLSI Journal**. Elsevier, Submitted on August 2021. **Status- with editor**. **(Indexed SCI-E IF: 1.211).**

M. Mohanraj, **P. Senthil**, "**Hybrid wave-pipelined adder**" 2016 International Conference on Computing for Sustainable Global Development (INDIA.Com) Pages: 1525 – 1527 **IEEE Conference**.
Link: https://ieeexplore.ieee.org/document/7724521

**PATENT- Published**
Title of Invention: **An Effective Method of Switching Activity Reduction in Multiplexer Using CanonicSigned Digit,** Application Number**: 201941028504 (U/S 11A), Publication Date: 02/08/2019**